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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,943	12/13/2004	Torayuki Tsukada	10921.0262USWO	3078

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EXAMINER	
HOANG, TU BA	

ART UNIT	PAPER NUMBER
2832	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/517,943	TSUKADA, TORAYUKI	
	Examiner	Art Unit	
	Tu Ba Hoang	2832	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

The title of the invention is too long.The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters. A new title is suggested. See 37 CFR 1.72(a) and MPEP § 606.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it should be limited to a single paragraph on a separate sheet. Correction is required. See MPEP § 608.01(b). It is noted that the disclosure of the invention should be directed to the technical aspect of the invention as a whole including a brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention. Thus, the technical aspect or objection should be clearly described and provided and shall not be referred to the claim. Therefore, the disclosure is objected to because of the following informalities: The use of phrases such as "according to claim 1", "According to claim 2", "According to claims 3 and 4", "According to claim 5", "According to claims 6 and 7" and so on as noted throughout the specification (from pages 4-12 of the DISCLOSURE section) should be removed or delected.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10, 12, and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "the metal layers" in line 4. There is insufficient antecedent basis for this limitation in the claim or from the preceding claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by JP-A-2002-57009 cited by the Applicant. JP-A-2002-57009 discloses a conventional structure, according to which a resistor element comprises a metal plate or rectangular chip formed of an alloy of low-resistant metal such as copper and high-resistant metal such as nickel.
The lower surface of the resistor element has lengthwise-spaced ends to which connection terminals are attached, the terminals being made of a metal having a lower resistance than the alloy making the resistor element. The surfaces of the connection terminals are formed with metal-plated layers for facilitating soldering to e.g. a printed circuit board (as described on the last paragraph on page 3 of the specification of the instant application).

Claims 1-20 are rejected under 35 U.S.C. 102(d) as being anticipated by Tsukada (JP2004-22658) which has the publication date on January 22, 2004. JP2004-22658 shows a chip resistor having low resistance and method of making thereof, comprising: a resistor element 2 formed of an alloy of high-resistant metal and low-resistant metal into a rectangular solid or rectangular prism; and connection terminal electrodes (shown in Figure 3) formed at ends of the resistor element ; wherein a surface of the resistor element is formed with a plating layer 5 made of pure metal with resistance lower than that of the alloy making the resistor element (see translation of the abstract), the alloy making the resistor element has a negative temperature coefficient of resistance, the resistor element is formed with a sectional area reducing portion, the sectional area reducing portion being filled with the plating layer as shown at least in Figures 1 and 5, the plating layer 5 on the surface of the resistor element is divided between the connection terminal electrodes 3, or is narrowed at least partially between the connection terminal electrodes as shown in Figure 4, the connection terminal electrodes 3 are integrally extended from ends of the resistor element 2 toward a lower surface of the resistor element, the plating layer being extended onto a surface of the extended electrodes as shown in Figures 1-5, metal plates serving as connection terminal electrodes 3 are fixed to ends of the lower surface of the resistor element 2, and wherein an insulator 4 covers an upper surface of the resistor element 2 with the plating layer 5, while also covering a portion between the connection terminal electrodes 3 on the lower surface of the resistor element 2 or at least the lower surface of the resistor element 2 except for ends thereof is covered by an insulator 4, the lower surface of the resistor element 2 being formed with a metal plating layer 5' disposed at the ends non-covered by the insulator as shown in Figure 5 with the metal layers 3 or 13 serving as the connection terminal electrodes of the resistor element as shown in Figures 4, 5, and 10-11 where the metal layers 3 or 13 can be formed at the ends of the lower surface and have a thickness equal to or larger than a thickness of a portion of the insulator covering the lower surface of the resistor

element as shown in Figures 13 and 19, wherein the upper surface and right and left side surfaces of the resistor element can also be covered by an insulator 4 as shown in Figures 10 and 11.

Regarding claims 16 and 20, the JP2004-22658 further discloses the method of making the chip resistor thereof where a lead frame A as shown in Figure 8 can be prepared and integrally formed with a plurality of lead bars A1 for forming resistor elements, the preparation using an alloy plate of high-resistant metal and low-resistant metal for forming a pure metal plating layer on a surface of the resistor element in each bar of the lead frame as shown in Figures 10-11, the resistance of the resistor element in each bar of the lead frame can be adjusted by trimming the groove 6 as shown in Figures 1, 3-6 and 9 and the resistor element in each bar off the lead frame can be cut after an insulator 4 for covering the resistor element is formed as shown in Figure 11.

Regarding claim 17, JP2004-22658 also discloses other method of making a chip resistor having low resistance, where a laminated material metal plate B is prepared by fixing a resistor element alloy plate B1 and a connection terminal electrode metal plate B2 to each other, the alloy plate is made of an alloy composed of high-resistant metal and low-resistant metal and is formed integral with a plurality of resistor elements 12 of a rectangular solid arranged, the connection terminal metal plate B2 is made of a metal having resistance lower than the alloy plate where at least portions of the connection terminal electrode metal plate are removed so as to leave connection terminal electrodes 13 after a plating layer of pure metal is formed on an upper surface of the resistor element alloy plate in the laminated material metal plate, or the plating layer of pure metal can be formed on the upper surface of the resistor element alloy plate after portions of the connection terminal electrode metal plate in the laminated material metal plate are removed so as to leave connection terminal electrodes as shown in Figures 14-17, insulators 4 are formed for covering the upper surface of the alloy plate and a part of the lower surface of the connection terminal electrode metal plate other than the connection terminal electrodes as shown in Figures 18-19, and finally, the laminated material metal plate is cut into the resistor elements.

Regarding claims 18-19, JP2004-22658 also inherently discloses at least other methods, where such method includes the steps of: making a rectangular resistor element from a metal plate; forming a pure metal plating layer on a surface of the resistor element; forming an insulator for covering at least a lower surface of the resistor element at a portion other than ends thereof; and forming metal plating layers serving as connection terminal electrodes of the resistor element at ends of the lower surface of the resistor element which are non-covered by the insulator , or such method which includes the steps of: making a rectangular resistor element from a metal plate; forming a pure metal plating layer on a surface of the resistor element; forming insulators 14 for covering an upper surface, a lower surface, and right and left side surfaces of the resistor element except for ends of the lower surface as noted in Figure 12; and forming metal plating layer serving as connection terminal electrodes of the resistor element at the ends of the lower surface of the resistor element which are non-covered by the insulator as shown in Figures 12-13, and 18-19.

Claims 1-15 and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura et al (US 5,907,274). Kimura et al shows a chip resistor (Figures 1 and 3) having low resistance (as indicated in the abstract, line 3) and method of making thereof, comprising: a resistor element 3 formed of an alloy of high-resistant metal (i.e., nickel) and low-resistant metal (i.e., copper) into a rectangular solid made of copper nickel alloy; and connection terminal electrodes (5) formed at ends of the resistor element ; wherein a surface (i.e., at least end portions) of the resistor element 3 is formed with a plating layer 2 or 8 made of pure metal such as silver (column 4, line 2) or copper (column 8, lines 34-35) with resistance lower than that of the alloy making the resistor element noted in Table 1 in column 5 where the alloy making the resistor element has a negative temperature coefficient of resistance, the resistor element 3 is formed with a sectional area reducing portion (i.e., the end portions) as shown, the sectional area reducing portion being filled with the plating layer 8, the plating layer 8 on the surface of the resistor element is divided between the connection terminal electrodes 5, at least the connection terminal electrodes 5 are integrally extended from ends of the resistor element 3 toward a lower surface of the resistor element, the plating layer 2 or 8 being extended onto a surface of the extended electrodes as shown in Figures 1 and 3-5, metal plates or layers serving as connection terminal electrodes 5 are fixed to ends of the lower surface of the resistor element 2, and wherein an insulator 4 covers an upper surface of the resistor element 3 with the plating layer 2 or 8, while also covering a portion between the connection terminal electrodes 5 on the lower surface of the resistor element 3 or at least the lower surface of the resistor element 3 except for ends thereof is covered by an insulator 4 (i.e., including the upper inner sides), the lower surface of the resistor element 2 being formed with a metal plating layer 8 disposed at the ends non-covered by the insulator as shown with the plating layers 2 or 8 also serving as the connection terminal electrodes of the resistor element, where the plating layers 8 can be formed at the ends of the lower surface and have a thickness equal to or larger than a thickness of a portion (i.e., the end portions) of the insulator 4 covering the lower surface of the resistor element 3, wherein the upper surface and right and left side surfaces of the resistor element can also be covered by the insulator 4 as shown.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Palanisamy (US 5,164,698) and Komeda (US 6,144,287).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu Ba Hoang whose telephone number is (571) 272-4780. The examiner can normally be reached on Mon-Thu from 6:00AM to 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on (571) 272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tu Ba Hoang
Primary Examiner
Art Unit 2832

September 20, 2006